

What is claimed is:

1. A pixel circuit for liquid crystal display for lowering power consumption via combining an analogue and a digital circuit, the circuit comprises:
 - a plurality of multiplexers, acting as switching elements for performing a plurality of output voltage transforming functions.
 - a thin film transistor, for connecting a scanning line and a data line, acting as a control switch of the circuit; and
 - a capacitor, connecting to the thin film transistor, where analogue or digital signals from the data line are stored.
2. The pixel circuit for liquid crystal display of claim 1, wherein said plurality of multiplexers comprises a first multiplexer and a second multiplexer.
3. The pixel circuit for liquid crystal display of claim 2, wherein said first multiplexer further comprises a general voltage terminal and a reference voltage terminal.
4. The pixel circuit for liquid crystal display of claim 2, wherein said second multiplexer further comprises:
 - a selection terminal;

- an output terminal;
- a first mode terminal; and
- a second mode terminal.

5. The pixel circuit for liquid crystal display of claim 4, wherein said second multiplexer further connects to a mode terminal.
6. The pixel circuit for liquid crystal display of claim 4, wherein said output terminal further connects to a liquid crystal unit.
7. The pixel circuit for liquid crystal display of claim 4, wherein said first mode terminal further connects to the capacitor and the thin film transistor.
8. The pixel circuit for liquid crystal display of claim 4, wherein the second mode terminal further connects to the output terminal of the first multiplexer.
9. A pixel circuit for liquid crystal display for lowering power consumption via combining an analogue and a digital circuit, the circuit comprises:
 - a plurality of multiplexers, acting as switching elements for performing a plurality of output voltage transforming functions.
 - a thin film transistor, for connecting a scanning line and a data

line, acting as a control switch of the circuit; and
a capacitor, connecting to the thin film transistor, where
analogue or digital signals from the data line are stored; and
a first switch device, for connecting said plurality of
multiplexer and a liquid crystal unit.

10. The pixel circuit for liquid crystal display of claim 9, wherein
said plurality of multiplexers comprises a first multiplexer and
a second multiplexer.

11. The pixel circuit for liquid crystal display of claim 10, wherein
said first multiplexer further comprises a general voltage
terminal and a reference voltage terminal.

12. The pixel circuit for liquid crystal display of claim 10, wherein
the second multiplexer further comprises:

a selection terminal;
an output terminal;
a first mode terminal; and
a second mode terminal.

13. The pixel circuit for liquid crystal display of claim 12, wherein
said second multiplexer further connects to a mode terminal.

14. The pixel circuit for liquid crystal display of claim 12, wherein the output terminal further connects to the first switch device.
15. The pixel circuit for liquid crystal display of claim 12, wherein the first mode terminal further connects to the liquid crystal unit.
16. The pixel circuit for liquid crystal display of claim 12, wherein the second mode terminal further connects to the first multiplexer.